REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	18 MAR 98	Final Technical Report: 29 SEP 97 - 28 MAR 98

4. TITLE AND SUBTITLE
Nanoelectronic Modeling Software Development

5. FUNDING NUMBERS
DAAH01-97-C-R276

6. AUTHOR(S)
William C.B. Peatman, President

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Advanced Device Technologies, Inc.
2015 Ivy Road, Ste. 308
Charlottesville, VA 22903

8. PERFORMING ORGANIZATION REPORT NUMBER
D1-031898

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Commander, U.S. Army Aviation and Missile Command
ATTN: AMSAM-RD-WS-DP-SB (Mr. Neal, Tech Monitor)
Bldg 7804, Room 213
Redstone Arsenal, AL 35898-5248

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. ABSTRACT *(Maximum 200 words)*

As the integration density of Very Large Scale Integrated Circuits (VLSICs) increases, conventional device technologies are becoming limited by switching speed, power dissipation, and interconnect capacitance. Alternatively, resonant tunneling diodes (RTDs) may extend the high speed, low power performance of nanoelectronic scale ICs, particularly when combined with highly functional, compact ultra low power switching devices such as the novel 2-dimensional MESFET (2-D MESFET). This project has lead to new device models (multi-gate 2-D MESFET) which, together with an accurate RTD model previously developed, have been implemented into a circuit simulator package which allows detailed studies of nanoelectronic ICs using these alternative device technologies.

14. SUBJECT TERMS	15. NUMBER OF PAGES
Low Power Electronics, Field Effect Transistors, Integrated Circuits 2-D MESFET, Resonant Tunneling, Modeling, Simulation	15
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

Nanoelectronic Modeling Software Development

March 18, 1998

Sponsored by Defense Advanced Research Projects Agency
(Controlling DARPA Office)

ARPA Order Nr. D611, Amdt 27

Issued by U.S. Army Aviation and Misslie Command Under

Contract Number: DAAH01-97-C-R276

Advanced Device Technologies, Inc.
2015 Ivy Road Ste. 308
Charlottesville, VA 22903

Dr. William C.B. Peatman
TEL: (804) 979-4103
FAX: (804) 979-2653
e-mail: 75033.206@compuserve.com

Contract Effective Date: 29 SEP 97

Expiration Date: 28 MAR 98

Nanoelectronic Modeling Software Development
Period: 1st Quarter 1998

Nanoelectronic Modeling Software Development
Contract Number: DAAH01-97-C-R276

PROJECT OBJECTIVE

This Phase I project has two primary objectives. The first objective is to develop an engineering model of Resonant Tunneling Devices (RTD) to be implemented in AIM-Spice, a commercial software package running under Windows 95/NT. The development of a reliable device model is a prerequisite for the design and production of any semiconductor device technology. The RTD model will be a semi-empirical, physics-based model which will be scalable, allowing the user to accurately simulate RTD circuits. The second technical objective of this project is to simulate RTD and RTD/FET circuits, such as inverters, memory elements, and analog-to-digital converters. One driving FET which we will examine closely is the heterodimensional 2-D MESFET, a novel side-gated FET which offers considerable promise for compact, ultra low power, multifunctional logic circuits. As part of this Phase I project, we will also refine the 2-D MESFET model already implemented in AIM-Spice in order to predict nanoscale 2-D MESFET device and circuit operation.

I. Introduction

New demands for integrated circuits (ICs) are emerging in areas that require high speed and low power concurrently, particularly for battery powered applications such as wireless communications and portable computing. As the number of transistors in Very Large Scale Integration (VLSI) continues to grow while the gate dimensions shrink, conventional technology— such as CMOS— is limited in terms of switching speed, power dissipation, and interconnect capacitance. In addition, cache memory continues to grow as more memory is integrated locally to processor cells, increasing the amount of layout area devoted to memory elements. Advances in semiconductor fabrication techniques and materials processing now permit novel nanoelectronic architectures with unique performance capabilities which address the limitations of conventional technologies. One example of these new architectures is the Resonant Tunneling Device. Resonant Tunneling Diodes, in particular, feature high speed, low capacitance, and material compatibility to conventional heterostructure FETs and HBTs. In addition, the NDR of the RTD load allows the design of inverters using only majority-carrier devices, with the benefits of simpler fabrication and high carrier mobility in both the switching and load devices. The requirement for fast operation with low-power dissipation in VLSI circuits suggests that the NDR of the RTD is an ideal inverter load element since it exhibits low current at digital logic levels for low static power but high current otherwise for high speed switching. Hence, highly functional, compact ultra low power logic elements are possible by integrating Resonant Tunneling Devices with high speed, low power compound semiconductor FETs, such as the novel heterodimensional 2-D MESFET [1-3].

A reliable device model is a prerequisite for the design and production of any semiconductor device technology. The flowchart shown in Fig. 1 illustrates how the device model is linked to all aspects of a given design process. For this DARPA Phase I SBIR project, we have implemented a physics-based engineering model of the Resonant Tunneling Diode in the commercial software simulator AIM-Spice. We have also refined the 2-D MESFET model already implemented in AIM-Spice in order to more accurately account for the dual-gate geometry of the device. Together, these two models allow for the simulation of compact, ultra low power, highly functional 2-D MESFET/RTD logic elements.

II. RTD Modeling

There are two approaches to modeling Resonant Tunneling Diodes: 1) numerical modeling, and 2) empirical modeling. To fully account for all physical mechanisms associated with the optical and transport properties of an RTD heterostructure, particularly for high frequency applications, numerical simulations are necessary. However, numerical simulations are computer and time intensive, so for applications in circuit simulators, physically-based analytical solutions are far more appealing. A number of empirical models for the RTD have been reported; however, most are basically analytical curve fitting procedures which are not based on the physics of the device (see, for example, [6, 7]). For example, the model developed by Robertson, et al, in [8], which was used by Advanced Device Technologies, Inc., in preliminary simulations of RTD/2-D MESFET logic elements, models the current-voltage characteristics of the RTD as a voltage controlled current source in parallel with a voltage-

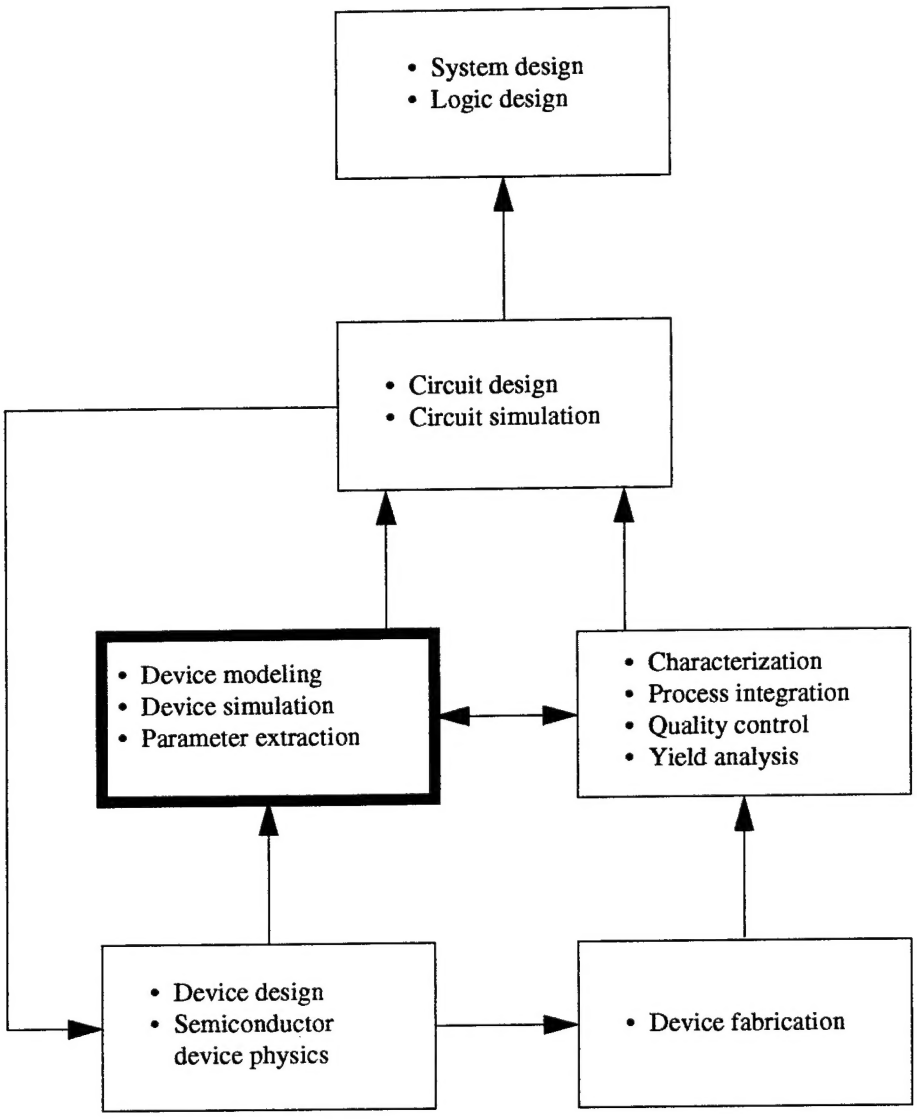

Fig.1. Flowchart of integrated circuit technological hierarchy (after [5], p. xiv).

shifted diode:

$$I = \frac{A_I V}{1 + A_V (V - V_{pe})^2} + V B_1 \exp\{B_2 (V - B_3)\} \tag{1}$$

where A_I, A_V determine the resonant peak current, V_{pe} is the peak voltage, B_1, B_2 determine the diode current, and B_3 represents the diode voltage shift.

There are two notable exceptions to the analytical approach: the models developed by Schulman, et al, in [9] and by E. R. Brown, et al, in [10]. In both of these cases, an analytic SPICE model for the current-voltage characteristics is developed from basic principles. Moreover, the Schulman model is widely accepted as the standard model for RTDs. Hence, for this DARPA Phase I project we implemented the Schulman RTD model into the circuit simulator AIM-Spice.

The Schulman model is derived from the quantum tunneling formalism for the current in the effective mass approximation:

$$J = \frac{em^*kT}{2\pi^2(h/(2\pi))^3}\int_0^\infty dET(E,V)\ln\left[\frac{1+e^{(E_F-E)/(kT)}}{1+e^{(E_r-E-eV)/(kT)}}\right] \tag{2}$$

where the transmission coefficient is approximated by a Lorentzian:

$$T(E,V) = \frac{\left(\frac{\Gamma}{2}\right)^2}{\left[E-\left(E_r-\frac{eV}{2}\right)\right]^2+\left(\frac{\Gamma}{2}\right)^2}. \tag{3}$$

Here, E is the energy measured up from the emitter conduction band edge, E_r is the energy of the resonant level relative to the bottom of the well at it's center, and Γ is the resonance width. By integrating (2) and applying several reasonable approximations described in [9], the following formula is obtained:

$$J_1(V) = A\ln\left[\frac{1+e^{(B-C+n_1V)\frac{e}{kT}}}{1+e^{(B-C-n_1V)\frac{e}{kT}}}\right]\left[\frac{\pi}{2}+\operatorname{atan}\left(\frac{C-n_1V}{D}\right)\right] \tag{4}$$

where A, B, C, D, H, n_1, and n_2 are fitting parameters. The valley current contribution is modeled by a simple diode,

$$J_2(V) = H\left(e^{n_2e\frac{V}{kT}}-1\right), \tag{5}$$

such that the total current is $J(V) = J_1(V) + J_2(V)$. Examples of AIM-Spice simulations of the Schulman model are shown in Fig. 2.

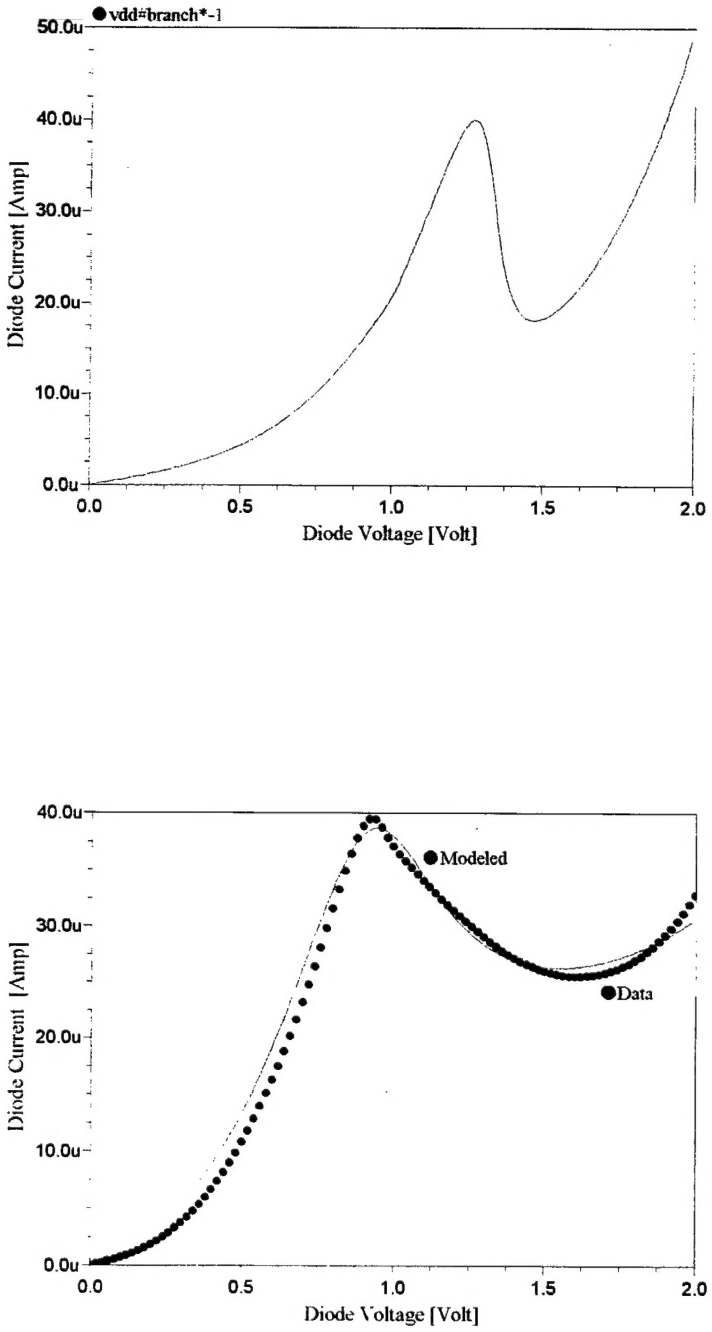

Fig.2. Examples of AIM-Spice simulations of the Schulman model.

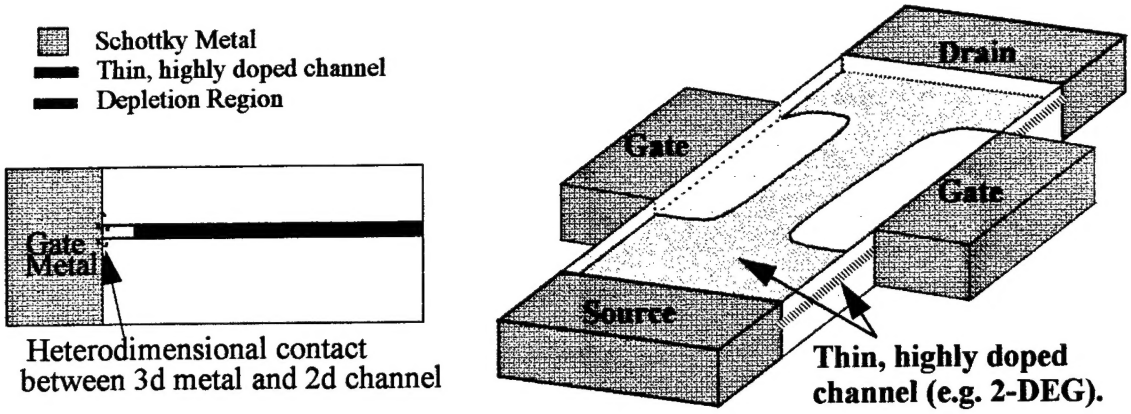

Fig.3. Schematic cross-section of the Schottky/2-dimensional electron gas junction (left) and perspective sketch of the 2-D MESFET (right) illustrating dual side gates which modulate the current flowing between the drain and source.

III. 2-D MESFET Model

An accurate analytical model for the current-voltage characteristics of the 2-D MESFET, based on the unified HFET model presented in [5], was presented in [1]. This model describes all operating regimes, including above and below threshold, using a single, continuous analytical equation. However, the model is essentially an empirical model and does not contain geometric-dependencies of parameters and is therefore not scalable. As part of this DARPA project, we have developed a more advanced 2-D MESFET model based on the physics of the device. In this new model, the parameters have a clear physical meaning and describe the geometric dependencies of the device. The model has been applied to three gate configurations: (1) the side gates are electrically tied together, (2) the dual side gates are biased independently, and (3) multiple (3 or more) gates are utilized in the same transistor. We have also developed an equivalent circuit model for the 2-D MESFET. In this circuit model, the device is split into several 2-D MESFETs, which are described using the unified single transistor model; hence, the complete model is also valid and continuous through all operating regimes.

The 2-D MESFET structure is shown in Fig. 3. The device is based on the lateral 3-D Schottky metal/2-D electron gas junction. The Schottky side gates laterally modulate the depletion width of the 2-DEG channel and thereby control the current between source and drain. The current-voltage characteristics of the 2-D MESFET can be modeled in an analogous way to HFETs [5]. Hence, the drain current of the unified 2-D MESFET is given by the expression:

$$I_d = \frac{g_{ch} V_{ds}(1+\lambda V_{ds})}{\left[1+\left(\frac{V_{ds}}{V_{sate}}\right)^m\right]^{1/m}}, \tag{6}$$

where V_{ds} is the drain-source voltage, I_{sat} is a unified expression of the saturation current, λ is the output conductance parameter, m is a knee-shape fitting parameter, and g_{ch} is the extrinsic conductance given by:

$$g_{ch} = \frac{g_{chi}}{1+g_{chi}(R_s+R_d)}. \tag{7}$$

Here $g_{chi} = \frac{qn_l\mu_n}{L}$, μ is the electron mobility, and n_l is the electron sheet charge density per unit length given by:

$$n_l = \frac{n'_l}{\left[1+\left(\frac{n_l}{n_{max}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}}, \tag{8}$$

where n_{max} is the maximum electron sheet density per unit length, γ is a fitting parameter, and n_l' is given by an approximate solution of the unified charge control model [6]:

$$n'_l = \frac{2c_{eff}\eta V_{th}}{q}\ln\left[1+\frac{1}{2}\exp\left(\frac{\left(\frac{V_{gs1}+V_{gs2}}{2}\right)-V_T}{\eta V_{th}}\right)\right]. \tag{9}$$

Here η is the subthreshold ideality factor, V_{th} is the thermal voltage, and c_{eff} is considered as a capacitance fitting parameter. The terms V_{gs1} and V_{gs2} account for the dual gate inputs.

The saturation current is written as [1]:

$$I_{sat} = \frac{g_{chi}V_{gte}\zeta}{\left(1+g_{chi}R_s+\sqrt{1+2g_{chi}R_s+\left(\frac{V_{gte}}{V_L}\right)^2}\right)(1+t_cV_{gte})}, \tag{10}$$

where ζ is the transconductance expansion factor, t_c is the transconductance compression factor, and $V_L=F_sL$ with F_s with being the saturation field. The effective gate voltage swing, V_{gte}, is

related to the gate-source voltage, V_{gs}, and the threshold voltage V_T as follows:

$$V_{gte} = V_{th}\left[1 + \frac{V_{gt}}{2\eta V_{th}} + \sqrt{\delta^2 + \left(\frac{\left(\frac{V_{gs1} + V_{gs2}}{2}\right) - V_{gt}}{2\eta V_{th}} - 1\right)^2}\right], \tag{11}$$

where the parameter δ determines the width of the transition between below and above threshold. Please note that (11) represents the equation used in [1] where we replaced V_{th} with ηV_{th}.

This HFET-like model is accurate for relatively long-channel devices. In short-channel devices the extension of the effective gate length caused by the depletion region has to be taken into account. We can model this effect by assuming an effective channel length that is equal to the gate length, L, increased by the length of the depletion extensions, the maximum value of which is d_{dep}. We write $d_{dep} = 2\varepsilon\frac{V_{bi} - V_{GS}}{qn_s}$ (α being a fitting parameter) since this effective channel length decreases with the increasing gate voltage. Therefore, in the model equations the channel conductance should be replaced by:

$$g_{chi} = \frac{qn_l\mu_n}{L + \alpha d_{dep}}. \tag{12}$$

We expect that in short-channel devices the dependence of the channel current on the gate voltage will deviate from linearity because of the second term in the denominator of the above expression. Previously, a different and empirical expression of n_l was used to fit the channel current measurements of submicron 2-D MESFETs [1]; n_l was assumed to be proportional to V^2_{gte} in the linear regime. No explanation was given but it was actually an empirical way to account for the dependence of the channel length on the gate voltage.

There is also a lower limit for the effective channel length, since d_{dep} cannot be smaller than zero. The lower limit of the channel length is related to the upper limit for the sheet charge density, and this effect can be included by expressing the depletion depth in terms of as:

$$d_{dep} = \frac{1}{2}\left(W_m - \frac{n_l}{n_s}\right). \tag{13}$$

The above expression tends to the appropriate limits in all operating regimes.

The dual-gate 2-D MESFET model also has to account for the nonlinear coupling between the gates that has been found in experimental measurements. This effect can be attributed to two facts: (1) the asymmetry of the two depletion extensions, and (2) to nonlinear

corrections on the relationship between depletion charge and gate voltage. This nonlinear coupling can be empirically modeled as a change in the threshold voltage:

$$\Delta V_T = \xi(V_{G1} - V_{G2})^2. \tag{14}$$

In a dual-gate device, we have modeled the effect of the dependence of channel length on the gate voltages by considering an average effective channel length. The resulting channel conductance is written as:

$$g_{chi} = \frac{qn_l\mu_n}{L + \alpha\left(\frac{d_{dep}}{L}\right)}, \tag{15}$$

where $d_{dep} = \frac{(d_{dep1} + d_{dep2})}{2}$.

To model multiple-gate (three or more gates) 2-D MESFETs we split the device into several dual-gate transistors. In Fig. 4 we see the structure of a 3-gate 2-D MESFET. For the corresponding circuit model, the device is split into two dual-gate 2-D MESFETs, each one modeled using the unified model described above.

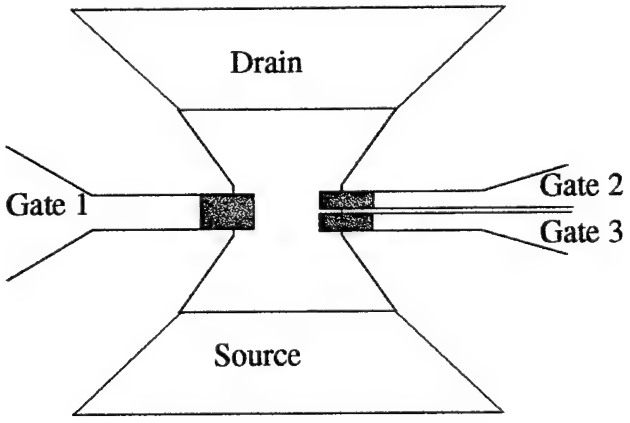

Fig.4. Top view of a 2-D MESFET having three gates.

We have validated the new model by comparison with experimental results for 2-D MESFET devices having different geometries. The devices were fabricated on a pseudomorphic heterostructure grown on a semi-insulating GaAs substrate. The parameter extraction procedures follow basically the methods reported in [5] for HFETs. In order to determine an unambiguous value of the threshold voltage, its extraction is carried out from the drain current vs. gate-source voltage characteristics by applying the same voltage at both gates.

In Figs. 5 and 6, we compare the measured and modeled characteristics of a three-gate 2-D MESFET at different bias conditions. The nominal gate length is 2.0 um and the maximum width is 1.0 um. In Fig. 5 (top) the device two gates are electrically tied together. In Fig. 5 (bottom), $V_{gs2} = V_{gs3} = 0.6$ V and we sweep V_{gs1}, so the device is working as a dual-gate device. In Fig. 6 $V_{gs1} = -1.2$ V, $V_{gs3} = 0.6$ V and we sweep V_{gs2}. The agreement is good in all bias conditions, even near the threshold voltage.

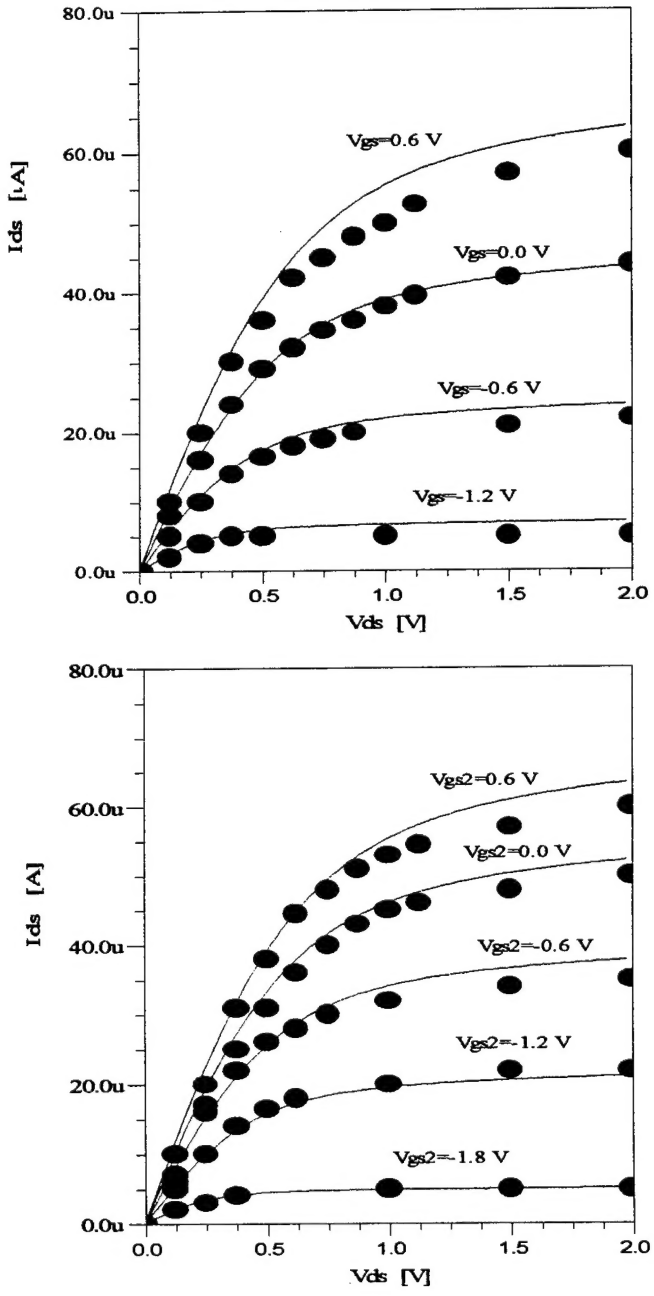

Fig.5. I_D vs. V_{ds} for a three-gate 2-D MESFET with L = 2 μm: (top) $V_{gs} = V_{gs1} = V_{gs2} = V_{gs3}$ and (bottom) $V_{gs1} = V_{gs3} = 0.6$ V.

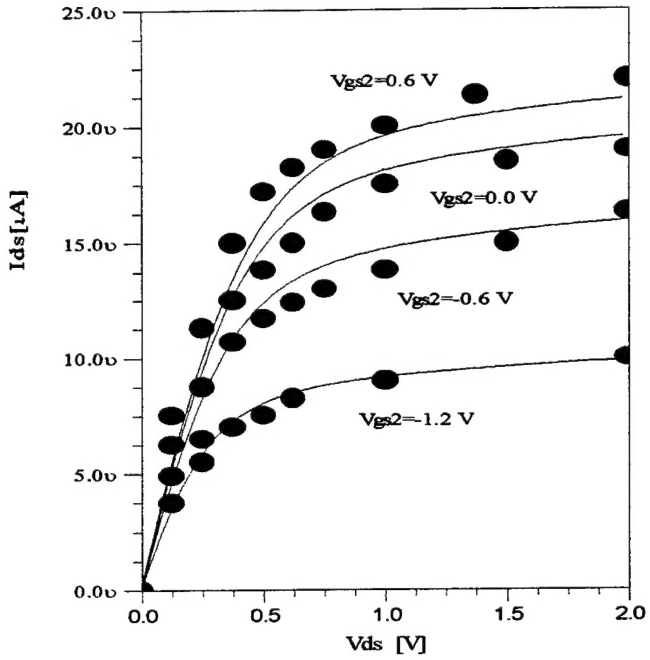

Fig. 6. I_D vs. V_{ds} for a three-gate 2-D MESFET with L = 2 μm and V_{gs1} = -1.2V and V_{gs3} = 0.6 V.

IV. RTD/2-D MESFET Circuits

Fig. 7 demonstrates a 2-D MESFET/RTD inverter. The transfer characteristics in the figure are for three different bias values on the second gate of the device while the first gate is swept as the input voltage, demonstrating the dual gate functionality of the 2-D MESFET. (The voltages at which the inverter switches are observed to vary as a function of the voltage applied to the second gate.) Such a logic element could be used, for example, as a sample-and-hold element with a programmable switching point.

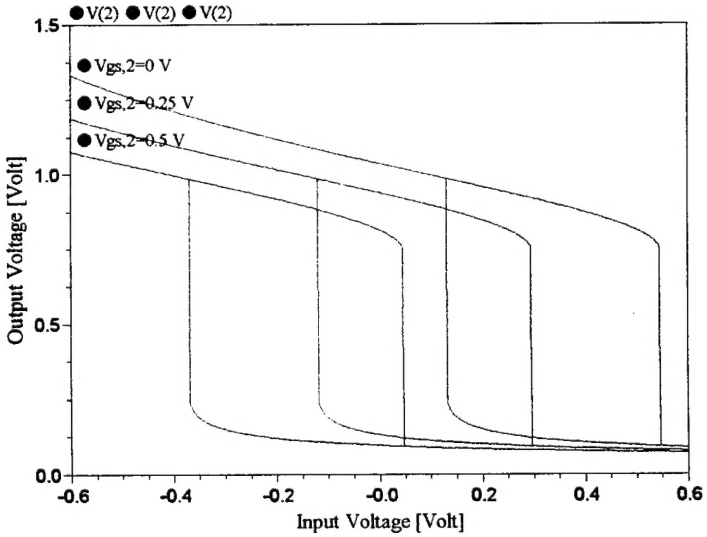

Fig. 7. RTD/2-D MESFET logic element utilizing dual-gate functionality of the 2-D MESFET for applications such as a sample-and-hold element with a programmable switching point.

References

[1] W. C. B. Peatman, M. Hurt, H. Park, T. Ytterdal, R. Tsai, and M. Shur, "Narrow Channel 2-D MESFET for Low Power Electronics," *IEEE Transactions on Electron Devices*, Vol. 42, No. 9, pp. 1569-1573, Sept. 1995.

[2] W. C. B. Peatman, H. Park, and M. Shur, "Two-dimensional metal-semiconductor field effect transistor for ultra low power circuit applications," *IEEE Electron Device Letters*, Vol. 15, No. 7, pp. 245-247, July 1994.

[3] W. C. B. Peatman, R. Tsai, T. Ytterdal, M. Hurt, H. Park, J. Gonzales, and M. Shur, "Sub-Half-Micrometer Width 2-D MESFET," *IEEE Electron Device Letters*, Vol. 17, No. 2, pp. 40-43, Feb. 1996.

[4] AIM-Spice World Wide Web page, http://www.aimspice.com.

[5] K. Lee, M. Shur, T. A. Fjeldly, and T. Ytterdal, Semiconductor Device Modeling for VLSI, Prentice Hall, New Jersey, 1993.

[6] C. E. Chang, P. M. Asbeck, K.-C. Wang, and E. R. Brown, "Analysis of Heterojunction Bipolar Transistor/Resonant Tunneling Diode Logic for Low-Power and High-Speed Digital Applications," *IEEE Trans. on Elec. Dev.*, Vol. 40, No. 4, pp. 685-691, April 1993.

[7] Z. Yan and M. J. Deen, "New RTD Large-Signal DC Model Suitable for PSPICE," *IEEE Trans. on Computer-Aided Design of Int. Circuits and Sys.*, Vol. 14, No. 2, pp. 167-172, Feb. 1995.

[8] J. Robertson, T. Ytterdal, W. C. B. Peatman, R. Tsai, E. Brown, and M. Shur, "RTD/2-D MESFET Logic Element for Compact, Ultra Low-Power Electronics," *IEEE Transactions on Electron Devices*, Vol. 44, No. 7, pp. 1033-1039, July 1997.

[9] J. N. Schulman, H. J. De Low Santos, and D. H. Chow, "Physics-Based RTD Current-Voltage Equation," *IEEE Electron Device Letters*, Vol. 17, No. 5, pp. 220-222, May 1996.

[10] E. R. Brown, O. B. McMahon, L. J. Mahoney, and K. M. Molvar, "SPICE model of the RTD," *Elec. Letters*, Vol. 32, no. 10, pp. 938-940, May 9, 1996.

Distribution List

Copies	Receipient
2	Commander U.S. Army Aviation and Missile Command ATTN: AMSAM-RD-WS-DP-SB (Mr. Neal, Tech Monitor) Bldg 7804, Room 213 Redstone Arsenal, AL 35898-5248
1	Commander U.S. Army Aviation and Missile Command ATTN: AMSAM-RD-CS-R Redstone Arsenal, AL 35898-5240
1	Director U.S. Army Aviation and Missile Command ATTN: AMSAM-RD-WS Redstone Arsenal, AL 35898-5248
1	Director Defense Advanced Research Projects Agency ATTN: ETO (Lt. Col. Gernot Pomrenke) 3701 North Fairfax Drive Arlington, VA 22203-1714
1	Director Defense Advanced Research Projects Agency ATTN: OASB/ARPA Library 3701 North Fairfax Drive Arlington, VA 22203-1714
2	Defense Technical Information Center ATTN: Acquisitions/OCP 8725 John J. Kingman Rd., STE 0944 Ft. Belvoir, VA 22060-6218
1	Director Defense Advanced Research Projects Agency ATTN: OASB/SBIR 3701 North Fairfax Drive Arlington, VA 22203-1714
1	Administrative Contracting Officer * DCMAO Baltimore ATTN: Chesapeake 200 Towsontown Blvd. West Towson, MD 21204-5299

* transmittal letter only, no report required to ACO.